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10/017,047	12/13/2001	Matthew A. Hayduk	42390P12401	6573

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EXAMINER	
ALI, SYED J	

ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,047	HAYDUK, MATTHEW A.	
	Examiner	Art Unit	
	Syed J Ali	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed August 9, 2004. Claims 1-27 are presented for examination.

2. The text of those sections of Title 35, U.S. code not included in this office action can be found in a prior office action.

Claim Rejections - 35 USC § 102

3. **Claims 1-3, 6-7, 10, 15-16, 18, and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Morozumi (USPN 6,570,571).**

4. As per claim 1, Morozumi teaches the invention as claimed, including an apparatus comprising:

a first processor to execute a first set of instructions (col. 2 lines 39-49);

a second processor to execute a second set of instructions (col. 2 lines 39-49);

a first monitor adapted to determine available performance capability of the first processor while executing the first set of instructions (col. 2 lines 50-59); and

a second monitor communicatively coupled to the first monitor and adapted to determine available performance capability of the second processor while executing the second set of instructions (col. 2 lines 50-59), wherein the apparatus is adapted to execute a third set of instructions on the first processor when the available performance capability of the second

processor is less than an acceptable performance level to execute the third set of instructions (col. 2 lines 60-65)

5. As per claim 2, Morozumi teaches the invention as claimed, including the apparatus of claim 1, further comprising memory to store the first, second, and third set of instructions (col. 3 lines 7-15).

6. As per claim 3, Morozumi teaches the invention as claimed, including the apparatus of claim 2, wherein the set of instructions comprise instructions of a program selected from the group consisting of an application program and an operating system program (col. 2 lines 36-49).

7. As per claim 6, Morozumi teaches the invention as claimed, including the apparatus of claim 1, wherein the first monitor is provided, at least in part, by a fourth set of instructions being executed on the first processor (col. 4 lines 10-16).

8. As per claim 7, Morozumi teaches the invention as claimed, including the apparatus of claim 6, wherein the first monitor is provided in part by logic circuitry within the first processor (col. 4 lines 10-16).

9. As per claim 10, Morozumi teaches the invention as claimed, including the apparatus of claim 1, wherein the acceptable performance level is defined by a user (col. 2 lines 50-59).

10. As per claim 15, Morozumi teaches the invention as claimed, including a method comprising:

polling a first processor to determine if the first processor has sufficient capacity to execute a first set of instructions when a second processor does not have sufficient capacity to execute the first set of instructions (col. 2 lines 50-59).

11. As per claim 16, Morozumi teaches the invention as claimed, including the method of claim 15, further comprising determining an available capacity of the second processor while the second processor is executing a second set of instructions (col. 2 lines 50-59).

12. As per claim 18, Morozumi teaches the invention as claimed, including the method of claim 15, further comprising determining if the capacity of the first processor is sufficient to execute the first set of instructions within a user defined performance level (col. 2 lines 50-59).

13. As per claim 24, Morozumi teaches the invention as claimed, including an article of manufacture comprising a storage medium having stored thereon instructions, that, when executed by a computing platform, results in:

polling a first processor to determine if the first processor has sufficient capacity to execute a first set of instructions when a second processor does not have sufficient capacity to execute the first set of instructions (col. 2 lines 50-59).

14. As per claim 25, Morozumi teaches the invention as claimed, including the article of claim 24, wherein the instructions, when executed, further results in:

determining if the capacity of the first processor is sufficient to execute the first set of instructions within a user defined performance level (col. 2 lines 50-59).

Claim Rejections - 35 USC § 103

15. **Claims 4-5, 22-23, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morozumi in view of Dean et al. (USPN 6,317,840) (hereinafter Dean).**

16. As per claim 4, Dean teaches the invention as claimed, including the apparatus of claim 1, wherein the first monitor is adapted to determine the available performance capacity based on a current operational voltage potential of the first processor (col. 1 line 55 - col. 2 line 12).

17. It would have been obvious to one of ordinary skill in the art to combine Morozumi and Dean since the method of load balancing performed by Morozumi is performed solely by an internal monitor calculating a threshold computational capacity. Dean, while providing a system that implements multiple functional units within a single processor, would provide a means of determining which of multiple processors is best suited to process any instruction. Specifically, Morozumi teaches the use of a manager to control the load balancing, which is similar in functionality to the control mechanism in Dean. To determine which processor is best suited to process an instruction, as in Dean, would have been an obvious modification to Morozumi, since it would allow the load balancing mechanism to be applied to any instruction.

18. As per claim 5, Dean teaches the invention as claimed, including the apparatus of claim 1, wherein the first monitor is adapted to determine the available performance capacity based on an operational frequency of the first processor (col. 1 line 55 - col. 2 line 12).

19. As per claim 22, Dean teaches the invention as claimed, including the method of claim 15, further comprising reducing the power consumption of the first processor if the first processor has excess capacity to execute a first set of instructions (col. 1 line 55 - col. 2 line 12).

20. As per claim 23, Dean teaches the invention as claimed, including the method of claim 22, further comprising reducing the voltage potential of the first processor (col. 1 line 55 - col. 2 line 12).

21. As per claim 27, Dean teaches the invention as claimed, including the article of claim 24, wherein the instructions, when executed, further results in:

reducing the power consumption of the first processor if the first processor has excess capacity to execute a first set of instructions (col. 1 line 55 - col. 2 line 12).

22. **Claims 8-9, 17, 19, 21, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morozumi in view of Blank et al. (USPN 6,496,823) (hereinafter Blank) in view of Chen et al. (US 2003/0012143) (hereinafter Chen).**

23. As per claim 8, Blank teaches the invention as claimed, including the apparatus of claim 1, wherein information about a system is used to perform predictive load balancing of work to be processed (col. 5 lines 12-27).

24. Chen teaches the invention as claimed, including the information about the system being maintained in a database to track an historical average of a processor demand needed to execute the third set of instructions (paragraph 0009).

25. It would have been obvious to one of ordinary skill in the art to combine Morozumi, Blank, and Chen since the load balancing mechanism of Morozumi only allocates tasks on a dynamic basis. A processor is prohibited from processing tasks if the processor has an insufficient capability to process the task. The command is thereafter sent to another processor. The method of Blank provides a mechanism that aids in the distribution of tasks by determining the available processing capacity, in terms of MIPS, of each processor in the system, as well as taking into account the processing speed of the processor. Thus, an initial load balancing can be performed. However, the method of predictive load balancing exhibited in Blank fails to take into account variations in demand from task to task. Rather, an assumption is made that each task to be processed puts the same workload upon the processor. Thus, a historical database for keeping track of past performance, as in Chen, would have been an obvious modification to Morozumi and Blank. Although Chen uses the historical database to monitor past performance based on users of a system rather than tasks, the predictive model is applicable to tasks as well, and can be used for dynamic allocation and reallocation of tasks among processors, in accordance with the methods of Morozumi and Blank.

26. As per claim 9, Blank teaches the invention as claimed, including the apparatus of claim 8, wherein the database includes an average million instructions per second [MIPS] to execute the third set of instructions (col. 6 lines 44-50).

27. As per claim 17, Blank teaches the invention as claimed, including the method of claim 16, wherein determining the available capacity of the second processor includes determining an available million instructions per second [MIPS] of the second processor (col. 6 lines 44-50).

28. As per claim 19, Chen teaches the invention as claimed, including the method of claim 18, further comprising determining historical average execution requirements for the first set of instructions (paragraph 0009).

29. As per claim 21, Blank teaches the invention as claimed, including the method of claim 19, further comprising storing the historical average execution requirements in a table (col. 5 line 62 - col. 6 line 5).

30. As per claim 26, Blank teaches the invention as claimed, including the article of claim 25, wherein the instructions, when executed, further results in:

determining historical average execution requirements for the first set of instructions (col. 5 line 62 - col. 6 line 5).

31. **Claims 11-14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morozumi in view of Conary et al. (USPN 5,842,029) (hereinafter Conary).**

32. As per claim 11, Conary teaches the invention as claimed, including the apparatus of claim 1, wherein the apparatus is adapted to increase the available performance capability of the second processor when the available performance capability of the first processor is less than the acceptable performance level to execute the third set of instructions on the first processor (col. 6 lines 9-32).

33. It would have been obvious to one of ordinary skill in the art to combine Morozumi with Conary since in cases where the load balancing mechanism of Morozumi determines that no processors are available to handle extra work, an alternative method of servicing the processing would be available. That is, if no processors can alleviate the processing load, the processor requesting assistance could utilize the method of Conary to increase the number of available processing cycles, thereby improving the performance of the processor. Furthermore, Conary provides the added benefit of allowing processors to go into a reduced power mode during periods of inactivity. This adds an extra dimension of efficiency to the overall system, while also implementing a dynamic load balancing technique.

34. As per claim 12, Conary teaches the invention as claimed, including the apparatus of claim 11, wherein the apparatus is adapted to increase the MIPS available on the first processor (col. 6 lines 9-32).

35. As per claim 13, Conary teaches the invention as claimed, including the apparatus of claim 11, wherein the apparatus is adapted to increase an operational voltage potential of the first processor (col. 15 lines 17-26).

36. As per claim 14, Conary teaches the invention as claimed, including the apparatus of claim 11, wherein the apparatus is adapted to increase an operational frequency of the first processor (col. 15 lines 17-26).

37. As per claim 20, Conary teaches the invention as claimed, including the method of claim 18, further comprising increasing the available capacity of the second processor if the capacity of the first processor is not sufficient to execute the first set of instructions within the user defined performance level (col. 6 lines 9-32).

Response to Arguments

38. Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new grounds of rejection.

Conclusion

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J Ali whose telephone number is (571) 272-3769. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Syed Ali
October 29, 2004

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